MEASUREMENT OF VOLTAGE, CURRENT AND FREQUENCY OF A CIRCUIT USING CRO	EXPTNO: 01
	DATE:

AIM : To understand the operation of the CRO and to learn how to determine the Amplitude

Time period and Frequency of a given signal using CRO.

APPARATUS:

S. No	Apparatus	Type	Range	Quantity
01	CRO			01
02	Function Generator		10-1MHz	01
03	Regulated Power supply		(0-30V)	01
04	Audio frequency probe			01

THEORY :CRO is an electronic device which is capable of giving a visual indication of a signal wave form. With an oscilloscope the waveform of the signal can be studied with respect to amplitude distortion and deviation from the normal. Oscilloscope can also be used for measuring voltage, frequency and phase shift. Cathode Ray Tube: Cathode Ray Tube is a heart of Oscilloscope providing visual display of the input signals. CRT consists of three basic parts.

1.Electron Gun. 2.Deflecting System. 3.Flouroscent Screen

These essential parts are arranged inside a tunnel shaped glass envelope

Electron Gun: The function of this is to provide a sharply focused stream of electrons. It mainly consists of an indirectly heated cathode, a control grid, focusing anode and accelerating anode. Control grid is cylinder in shape. It is connected to negative voltage w.r.t to cathode. Focusing and accelerating anodes are at high positive potential. w.r.t anode. Cathode is indirectly heated type & is heated by filament. Plenty of electrons are released from the surface of cathode due to Barium Oxide coating. Control Grid encloses the cathode and controls the number of electrons passing through the tube.

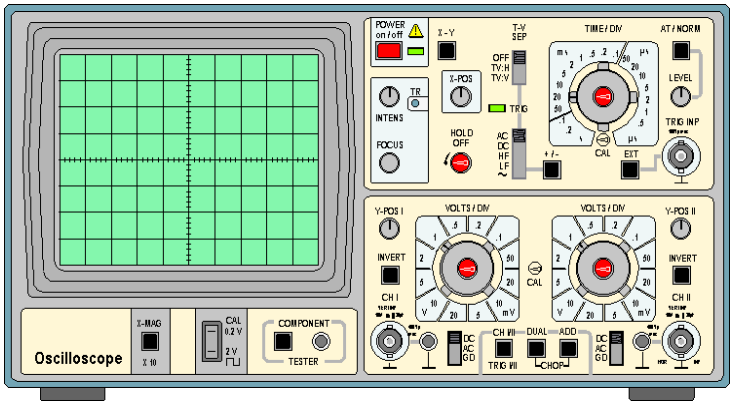
A voltage on the control grid consists the cathode determines the number of electrons freed by heating whichareallowedtocontinuemovingtowardsthefaceofthetube.Theacceleratedanodeisheatedat much higher potential than focusing anode. Because of this reason the accelerating anode accelerates the light beam into high velocity.Thebeamwhenstrikesthescreenproducesthespotorvisiblelight.

The name electron Gun is used because it fires the electrons like a gun that fires a bullet.

Deflection system: The beam after coming out of the accelerated anode passes through two sets of deflection plates with the tube . The first set is the vertical deflection plate and the second set is horizontal deflection plates. The vertical deflection plates are oriented to deflect the electron beam that moves vertically up and down. The direction of the vertical deflection beam is determined by the voltagepolarityappliedtotheplates.Theamountofdeflectionissetbythemagnitudeoftheappliedvoltage.The

beam is also deflected horizontally left or right by a voltage applied to horizontal plates. The deflecting beam is then further accelerated by a very high voltage applied to the tube.

Fluorescent Screen: The screen is large inside the face of the tube and is coated with a thin layer of florescent material called Phosphor. On this fluorescent material when high velocity electron beam strikes its converting the energy of the electron the electron beam between into visible light(spots). Hence the name is given as fluorescent screen.



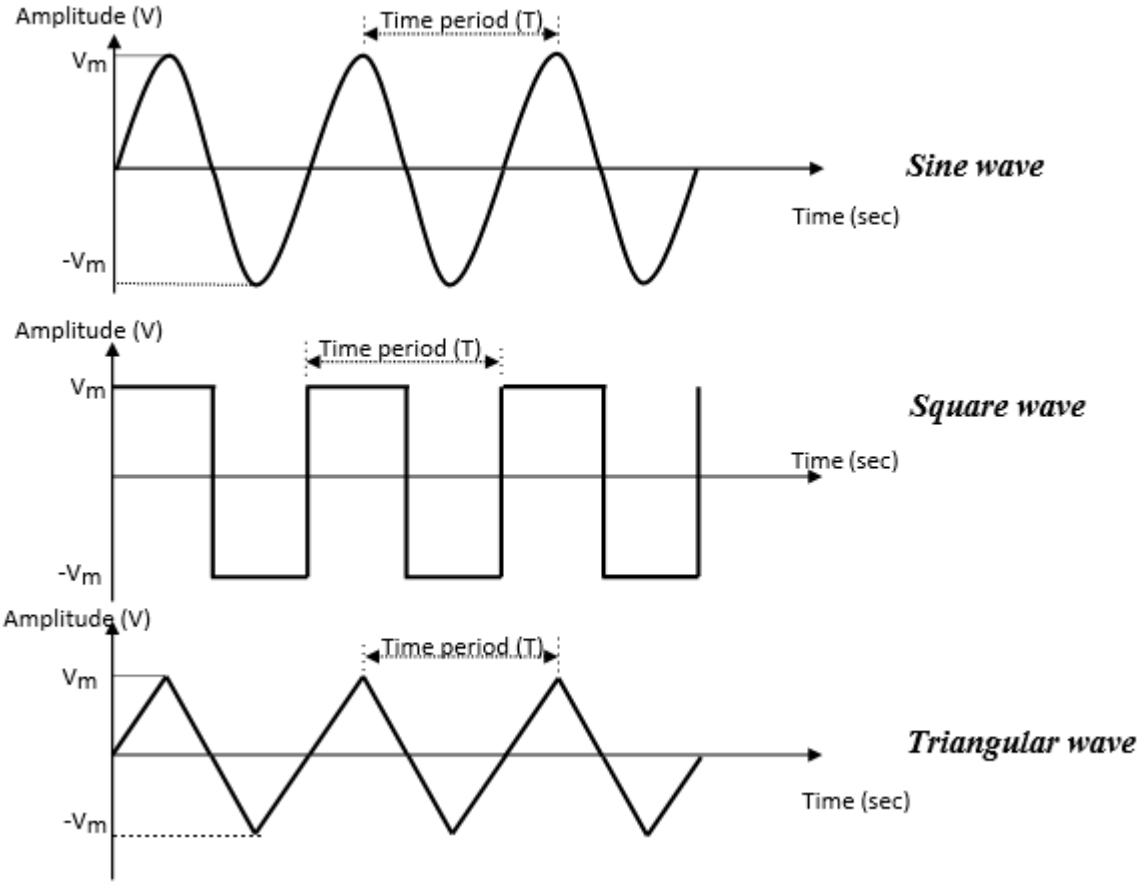
PROCEDURE:

1. Turn on the power of the CRO.
2. FromtheFunctionGeneratorselectthedesiredfrequencyandamplitudeofthesinewave.The amplitude of the waveform is obtained by noting the number of divisions along the Y-axis in between peak to peak of the waveform (i.e. sine waveform / Triangular waveform /Square waveform) and multiplying with the divisional factor of the amplitude note in volts.
3. Time period is calculated from X-axis.
4. Frequency is obtained by formula F=1/T.
5. This frequency is compared with the frequency applied using function generator.
6. Voltage in the CRO is compared with the voltage applied from function generator.
7. By repeating the above steps we can find frequency and voltages of square wave & triangular waveforms.

TABULAR COLUMN:

Waveform	Time Period(sec)		Frequency(Hz)		Amplitude(V)	
	Theoretical	Practical	Theoretical	Practical	Theoretical	Practical
Sinusoidal						
Triangular						
Square						

MODEL GRAPHS:



CALCULATIONS:

1. Sinusoidal Waveform:

Amplitude:_____V, Time Period: _____Sec, Frequency:_____Hz

2. Square Waveform:

Amplitude _____ V, Time Period: _____Sec, Frequency:_____Hz

3. Triangular Waveform:

Amplitude : _____ _____ V ,Time Period:_____ Sec, Frequency:____Hz

RESULT:

CRO Panel is studied and determined the Amplitude, Time period and Frequency of Signal.

Design of Clipper circuits using Diode.	EXPT NO:2
	DATE:

AIM: To design a series and shunt clipper to get a clip of voltage at output for a sinusoidal input Signal of respective peak to peak voltages.

APPARATUS REQUIRED: -

S. No	Apparatus	Specification	Quantity
1.	CRO (Dual Channel)	0 to 20 MHz	1
2.	Signal Generator	1Hz to 1 MHz	1
3.	Diode	1N4007	2
4.	Resistor	4.7 KΩ	2
5.	D.C Power Supply	(0 – 30 V (dual)	1
6.	Connecting wires	-----	1 Bunch
7.	Bread board	-----	1
8.	BNC cables	-----	2

THEORY:

The process whereby the form of sinusoidal signals is going to be altered by transmitting through a non-linear network is called non-linear wave shaping. Non-linear elements (like diodes, transistors) in combination with resistors can function as clipper circuits.

Clipping circuits are used to select transmission of that part of an arbitrary wave form which lies above or below some reference voltage level. Clipping circuits are also referred to as Limiters, Amplitude selectors or Slicers.

Clipping circuits are constructed using a combination of resistors, diodes or transistor and reference voltage. Clipping circuits are classified based on the position of diode as

i) Series diode clipper ii) Shunt diode clipper.

CIRCUIT DIAGRAM (Series Clipper):

A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the positive portions of the waveform, is termed as Positive Series Clipper.

When the input voltage is applied, the positive cycle of the input makes the point A in the circuit positive with respect to the point B as shown in Fig1. This makes the diode reverse biased and hence it behaves like an open switch. Thus the voltage across the load resistor becomes zero as no current flows through it and hence V0 will be zero.The negative cycle of the input makes the point A in the circuit negative with respect to the point B. This makes the diode forward biased and hence it conducts like a closed switch. Thus the voltage across the load resistor will be equal to the applied input voltage as it completely appears at the output V0.

A Clipper circuit in which the diode is connected in series to the input signal and biased with positive reference voltage Vr and that attenuates the positive portions of the waveform, is termed as Positive Series Clipper with positive Vr as shown in Fig2. The following figure represents the circuit diagram for positive series clipper when the reference voltage applied is positive. During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output. During its negative cycle, the diode gets forward biased and conducts like a closed switch. Hence the output waveform appears as shown in the above figure.

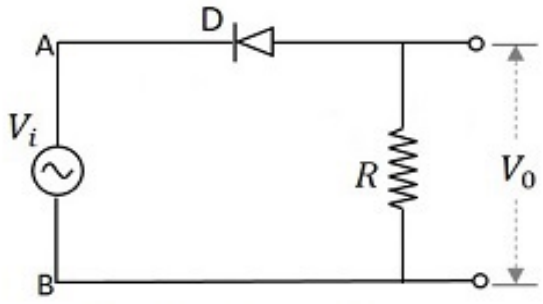


Fig1 Positive Series Clipper

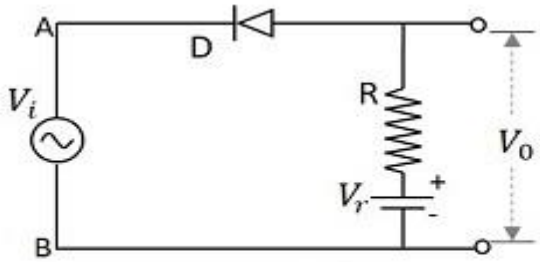
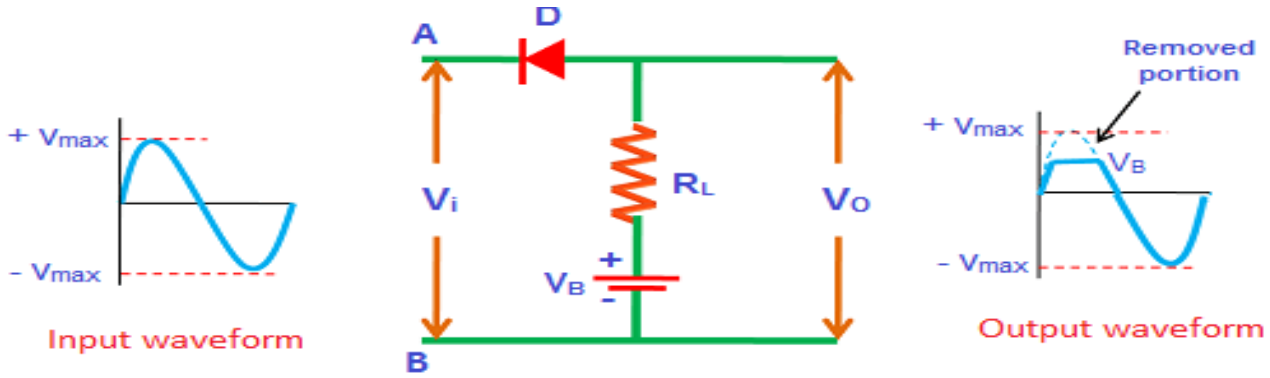


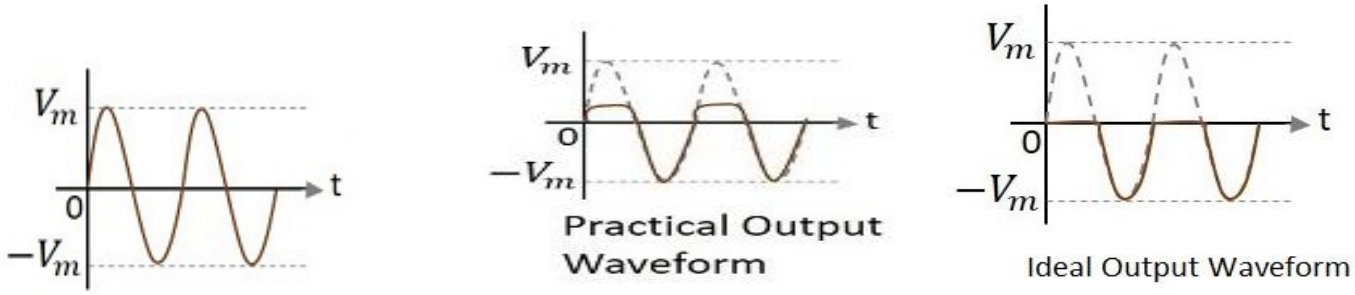
Fig2: Positive Series Clipper with positive V_r



Series positive clipper with positive bias

MODEL GRAPHS:

Input waveform: **Output Waveform:**



CIRCUIT DIAGRAM (Shunt Clipper):

In shunt clipper, the diode is connected in parallel with the output load resistance. The operating principles of the shunt clipper are nearly opposite to the series clipper. The shunt clipper on the other hand passes the input signal to the output load when the diode is reverse biased and blocks the input signal when the diode is forward biased.

CIRCUIT DIAGRAM (Shunt Clippers):

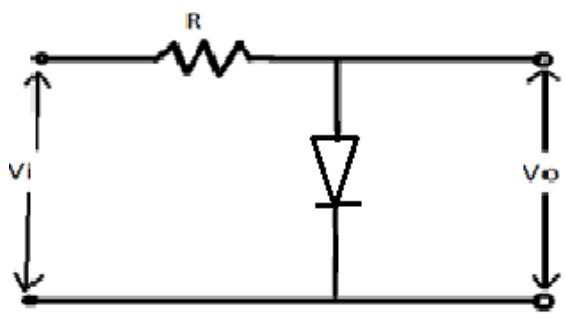


Fig1: **Unbiased Positive clipper**

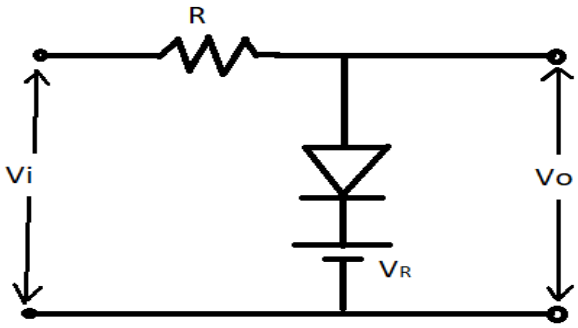


Fig2: **Positive clipper with positive reference**

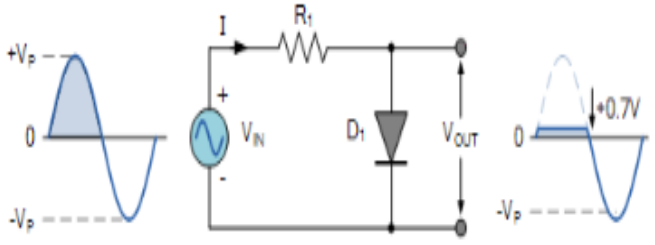


Fig3: Shunt positive clipper without bias

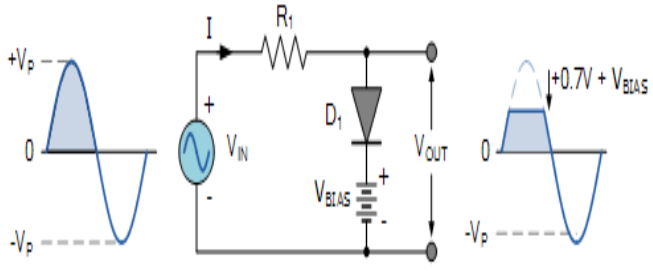
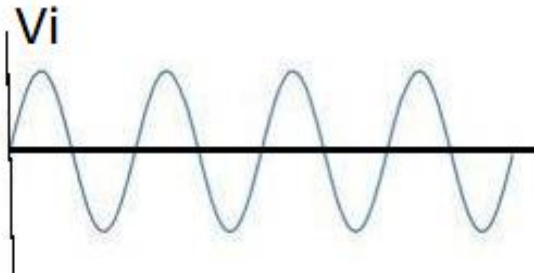


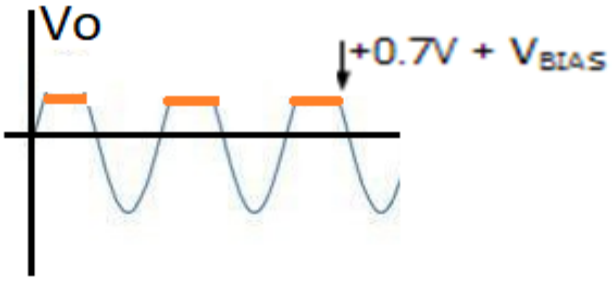
Fig4: Shunt positive clipper with bias

MODEL GRAPHS:

Input waveform:



Output waveforms:



PROCEDURE:

1. Connect the circuit as shown in the figures.
2. In each case, by applying different value of reference voltage change the peak voltage of input signal and note the theoretical and practical clipping values.
3. Observe the Output waveform (V_O in the circuit) on the CRO and compare it with theoretical values.
4. Sketch the Input as well as Output waveforms and mark the voltage levels.
5. Obtain the transfer characteristics of Clipper circuit, by keeping CRO in X-Y mode

PRECAUTIONS:

Set the CRO Output channel in DC mode always.

1. Observe the waveforms simultaneously in two channels by keeping the same reference ground.
2. See that there is no DC component in the INPUT.
3. To find transfer characteristics, apply input to the X-Channel, Output to Y-Channel, adjust the dot at the center of the screen when CRO is in X-Y mode. Both the channels must be in ground, then remove ground.

OBSERVATIONS:

S.No	V_R(in Volts)	Vm = V_R + V_γ+2v (Volts)	Theoretical clipping	Practical clipping
1				
2				
3				

VIVA QUESTIONS:

1. Define non linear wave shaping? What are the non-linear components?
2. Define clipping circuit? What are the other names for clippers?
3. Write the piecewise linear characteristics of a diode?
4. What are the different types of clippers?
5. Which kind of a clipper is called a slicer circuit?
6. What are the applications of Clipper Circuits?
7. What is the figure of merit for diodes used in clipping circuits?
8. What is the influence of the practical diode compared to the ideal diode, in the above circuits?
9. Instead of sinusoidal wave form as input, if we give other wave forms like triangular or square, then how the clipping action is performed?
10. What is V_γ for Ge diode and V_γ for Si diode?

RESULT*:*

The series and shunt clipper circuit is designed, compared the theoretical and practical values and observed the response for various combinations of V_R.

Design of Clamper circuit using Diode	EXPT NO: 3
	DATE:

AIM*:* To design a clamping circuit such that the positive peak of input signal is to clamp at ____V.

APPARATUS:

S.No	Apparatus	Specification	Quantity
1.	CRO (Dual Channel)	0 to 20 MHz	1
2.	Signal Generator	1Hz to 1 MHz	1
3.	Diode	1N4007	1
4.	Resistor	100 KΩ	1
5.	Capacitor	0.l µF	1
6.	D.C Power Supply	(0 – 30 V (dual)	1
7.	Connecting wires	-----	1 Bunch
8.	Bread board	-----	1
9.	BNC cables	-----	2

THEORY:

A clamper is an electronic circuit that changes the DC level of a signal to the desired level without changing the shape of the applied signal. In other words, the clamper circuit moves the whole signal up or down to set either the positive peak or negative peak of the signal at the desired level. The Clampers clamp the given waveform either above or below the reference level, which are known as positive or negative clampers respectively.

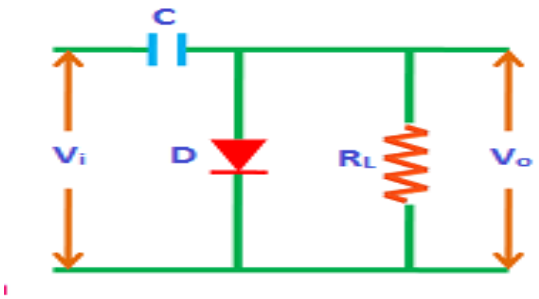
Clamping circuits are classified as two types.

i) Negative Clampers ii) Positive Clampers

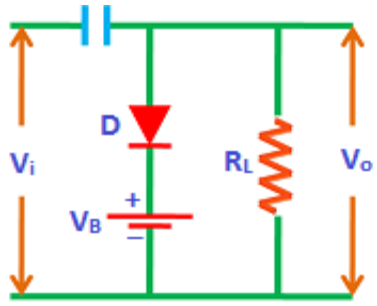
i.Negative Clamper: If the circuit pushes the signal downwards then the circuit is said to be a negative clamper. When the signal is pushed downwards, the positive peak of the signal meets the zero level.

ii.Positive Clamper: If the circuit pushes the signal upwards then the circuit is said to be a positive clamper. When the signal is pushed upwards, the negative peak of the signal meets the zero level.

CIRCUIT DIAGRAM (Negative Clamper**):**



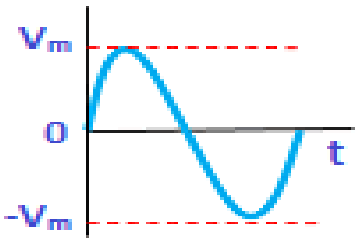
Negative clamper

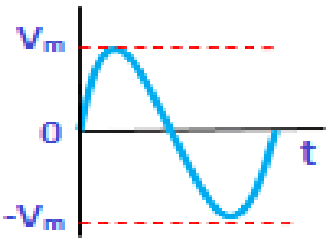


Negative clamper with positive bias

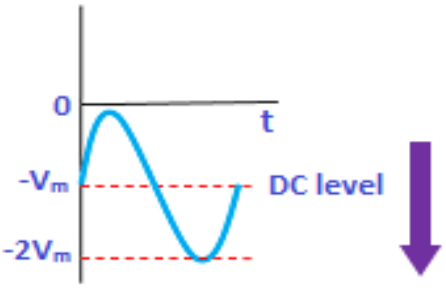
MODEL GRAPHS:

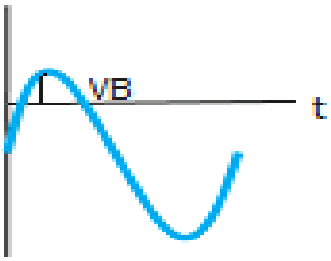
Input waveform:



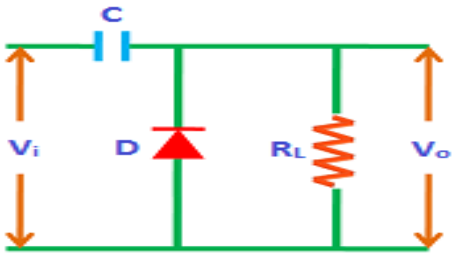


Output waveforms:

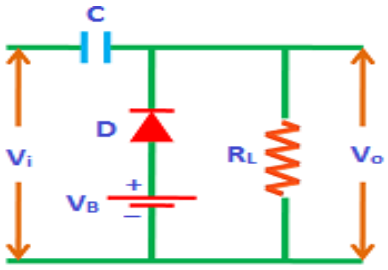




CIRCUIT DIAGRAM (Positive Clamper):



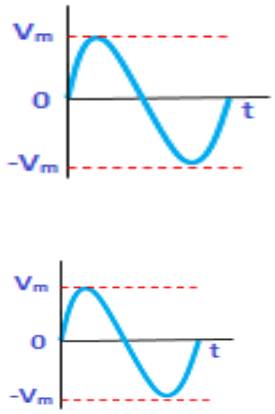
Positive clamper



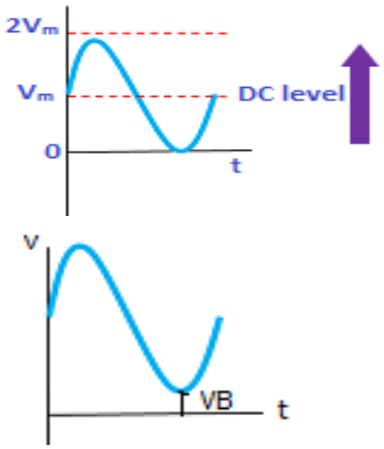
Positive clamper with positive bias

MODEL GRAPHS:

Input waveform:



Output waveforms:



PROCEDURE:-

l. Connect the circuit as shown in the figure above.
2. By apply above procedure calculate the required reference voltage. And repeat the experiment for different values of positive peak clamping value.
3. A Sine wave of l0V P-P, l KHz at the input terminals with the help of Signal Generator.
4. Observe the Input & Output waveforms on CRO and plot the waveforms and compare the theoretical and practical values.
5. Output is taken across the load RL.

PRECAUTIONS:

1. Set the CRO Output channel in DC mode always.
2. Observe the waveforms simultaneously in two channels by keeping the same reference ground.
3. See that there is no DC component in the INPUT.
4. To find transfer characteristics, apply input to the X-Channel, Output to Y-Channel, adjust the dot at the centre of the screen when CRO is in X-Y mode. Both the channels must be in ground, then remove ground and plot the transfer characteristics.

VIVA QUESTIONS:

1. What are the applications of clamping circuits?
2. What is the synchronized clamping?
3. What is the difference between a clipper and a clamper?
4. What are the other names for clampers?

RESULT:

The different types of clamping circuits are studied and the response was observed for various.

4.Estimation of ripple factor and regulation of rectifiers without and with LC filter	EXPT.NO:4(a)
	DATE:

AIM: To observe the input &output waveforms of Half-Wave Rectifier without and with LC filter. And to find the Ripple factor & Percentage of load Regulation.

APPARATUS:

1.Transformer 230v/6v–0–6v	-1No
2.Diodes IN4007	-1No
3.Decaderesistance Box	-1No
4.Multimeter	-1 No
5.BreadBoard	-1 No
6.20MHzDualTrace CRO	-1 No
7.Connecting wires	

THEORY:

As per the circuit diagram, it contains transformer an done diode, DRB, Capacitor. During the positive swing of

Power supply, the diode acts as forward bias condition. Hence it offers very less resistance. Thus whatever the input signal is applied transmitted to the load resistance when the negative swing of the A.C signal is applied to the diode, it acts as reverse bias connection Since it offers as high resistance. In this no signal is allowed to the load. Thus it gives Half wave output signal. The amount of A.C signal is present in output wave form is measured by ripple factor.

$$\text{Ripple factor} = \frac{V_{rms}}{V_{DC}} \qquad \text{Percentage of Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

CIRCIT DIGRAM :

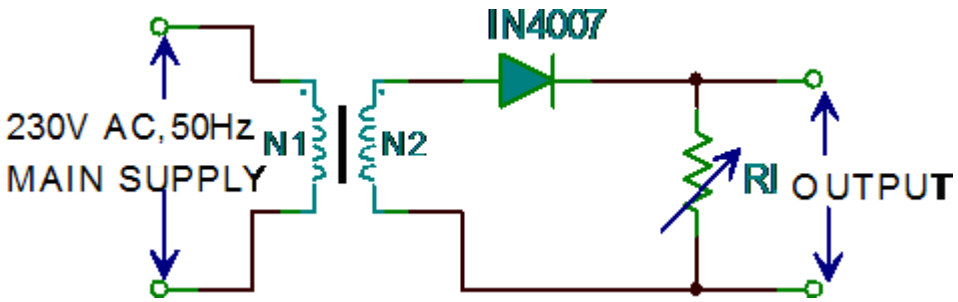


Fig: Half Wave Rectifier Without Filter

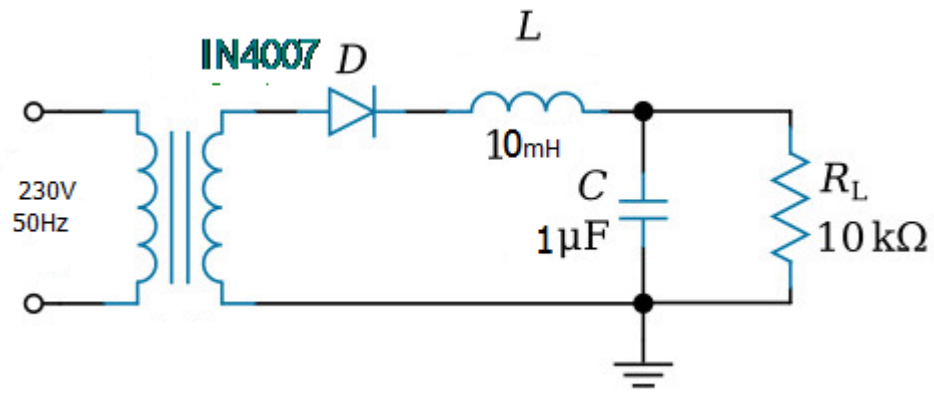


Fig: Half Wave Rectifier With LC Filter

PROCEDURE:

1. Connecting the circuit on breadboard as per the circuit diagram
2. Connecttheprimaryofthetransformertomainsupplyi.e.230V,50Hz
3. Connect the decade resistance box and set the RL value to 500Ω
4. Connect the Multi meter at output terminals and vary the load resistance(DRB) from500Ω to 5KΩ and note down the Vac and Vdc as per given tabular form
5. Disconnect load resistance(DRB) and note down No load voltage Vdc.
6. Connect load resistance at 5KΩand connect Channel–II of CRO at output terminals and CH–I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet
7. Calculate Ripple Factor $= \frac{Vac}{Vdc}$
8. Calculate Percentage of regulation $= \frac{Vnoload - Vfull\ load}{Vfullload} \times 100\%$

TABULAR FORM: Without filter

V no Load Voltage(Vdc)=

S.NO	Load Resistance In Ohms	Vdc (Volts	Vac (Volts)	Ripple Factor γ	% of Regulation $\frac{V_{NL}-V_{FL}}{V_{FL}} X100$
1	500				
2	5K				

TABULAR FORM: With filter

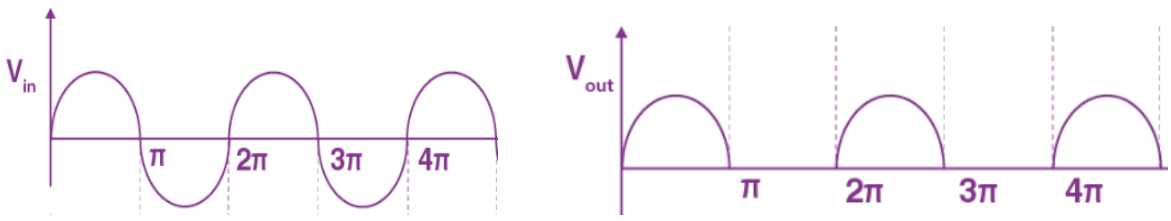
V no Load Voltage(Vdc)=

S.NO	Load Resistance In Ohms	Vdc(Volts)	Vac (Volts)	Ripple Factor γ	% of Regulation $\frac{V_{NL}-V_{FL}}{V_{FL}} X100$
1	500				
2	5K				

WAVESHAPES:

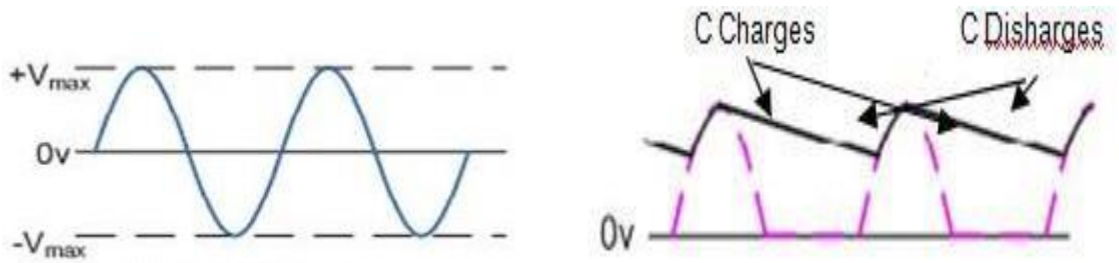
Half Wave Rectifier Without Filter:

Input Wave form **Output wave form**



Halfwave With LC Tfilter:

Input Wave form **Output wave form**



PRECAUTIONS:

1. Don’t touch the Primary side of the Transformer when it is PLUG-IN.
2. Maintain R_L(DRB)shouldbeabove100Ω.

RESULTS: Average Ripple factor without filter=

Average Ripple factor with filter=

Average Percentage of load Regulation without filter=

Average Percentage of load Regulation with filter =

Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Half wave rectifiers with & without filter.

VIVAQUESTIONS:

1. What is the function of half wave rectifier(HWR)?
2. What is meant by voltage regulation of HWR?
3. What are the applications of HWR?
4. What is the value of peak inverse voltage of HWR?
5. What is the value of ripple factor in HWR?

Estimation of ripple and regulation of rectifier with and without LC filter of Full wave rectifier	EXPT.NO:4(b)
	DATE:

AIM: To observe the input &output wave forms of Full- Wave Rectifier with and without filters. And to find the Ripple factor and Percentage of load Regulation.

APPARATUS:

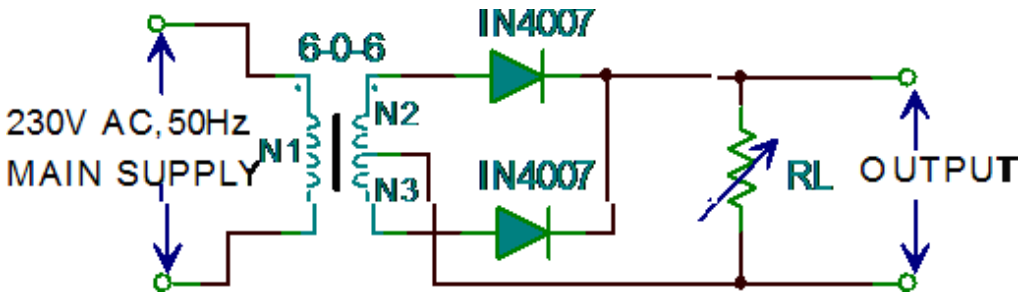
1.Transformer230v/6v–0–6v	-1 No
2.DiodesIN4007	-2Nos
3.Capacitor 470µf/35v	-1 No.
4.DecaderesistanceBox	-1No
5.Multimeter	-1No
6.BreadBoard	-1 No
7. 20MHzDualTrace CRO	-1 No

THEORY:

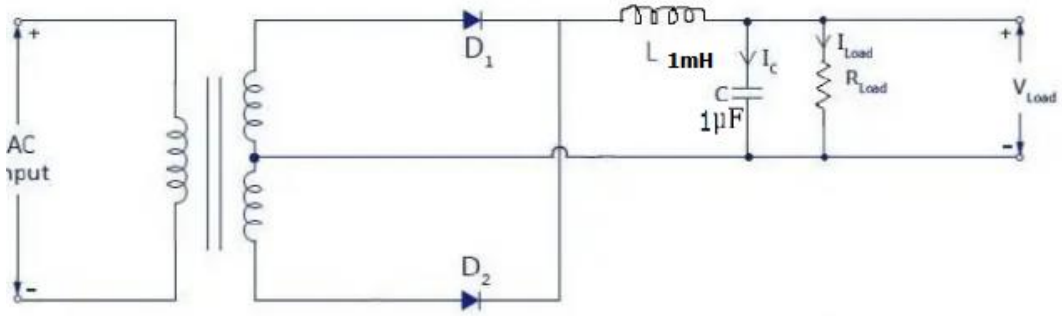
It contains two diodes connected across the load and a center tapped transformer. When the input is 0 to □ due to the center tapping we have two waveforms which are in opposite phase. Diode1 acts as a conductor in 0 to □. The diode 2 acts as a non-conductor. Hence the output is almost equal to input of diode 1.When the primary of transformer is between □ to 2□ diode 1 acts as non-conductor and diode 2 acts as conductor. Hence the output signal is almost equal to input signal of diode2 Thus we can observe a continuous waveform.

CIRCUITDIAGRAM:

FULLWAVEWITHOUTFILTER



FULLWAVE WITH LC FILTER



PROCEDURE:

1. Connecting the circuit on breadboard as per the circuit diagram.
2. Connect the primary of the transformer to mainsupplyi.e.230V,50Hz
3. ConnectthedecaderesistanceboxandsettheRLvalueto100Ω
4. Connect the multi meter at output terminals and vary the load resistance(DRB) from100Ω to 5KΩ and note down the $V_{ac}$and V_{dc}as per given tabular form
5. Disconnect load resistance(DRB)and note down No load voltage Vdc
6. Connect load resistance at 1KΩ and connect CH – I of Dual Trace CRO at Secondary(Input)terminals, Channel–II of Dual Trace CRO at output terminals and observe and note down the Input and Output Wave form on Graph Sheet
7. Calculate Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$
8. Calculate Percentage of regulation $= \frac{V_{no\ load} - V_{full\ load}}{V_{full\ load}} \times 100\%$

TABULARFORM: Without filter

V no Load Voltage(Vdc)=

S.NO	Load Resistance In Ohms(RL)	Vdc (Volts)	Vac(Volts)	Ripple Factor γ	% of Regulation $\frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$
1					
2					

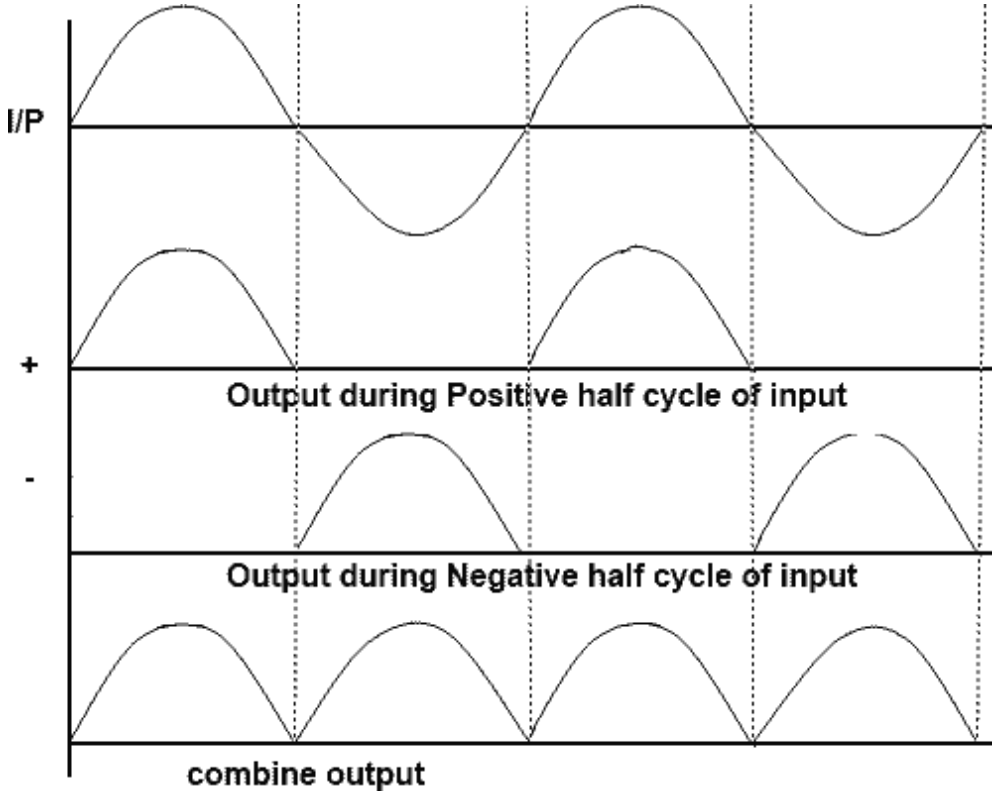
TABULAR FORM :With filter

V no Load Voltage(V_{dc})=

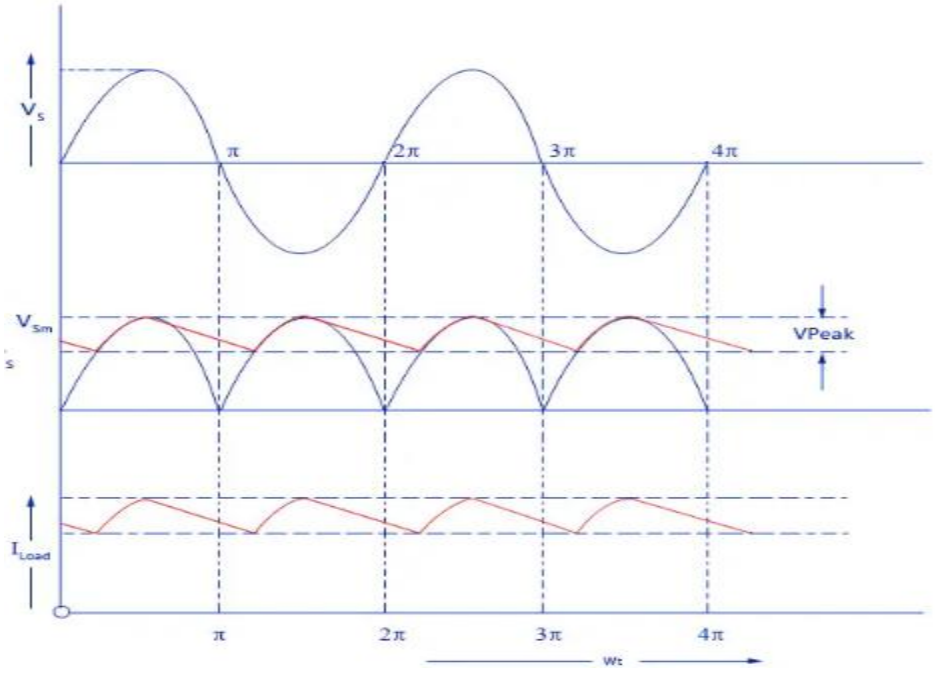
S .No	Load Resistance In Ohms	Vdc(Volts)	Vac(Volts)	Ripple Factor γ	% of Regulation $\frac{V_{NL}-V_{FL}}{V_{FL}} X100\%$
1	1K				
2	2K				

WAVESHAPES:

FULLWAVEWITHOUTFILTER



FULLWAVEWITHFILTER



PRECAUTIONS:

1. Don't touch the Primary side of the Transformer when it is PLUG-IN.
2. Maintain R_L(DRB)shouldbeabove100Ω.

RESULTS: Average Ripple factor without filter=

Average Ripple factor with filter =

Average Regulation without filter =

Average Regulation with filter=

Observe Input and Output Wave forms and Calculate ripple factor and percentage of regulation in Full wave rectifiers with & without filter

VIVAQUESTIONS:

1. What is the function of full-wave rectifier (FWR)?
2. What is meant by voltage regulation of FWR?
3. What are the applications of FWR?
4. What is the value of peak inverse voltage of FWR?
5. What is the value of ripple factor in FWR?

Determination of h-Parameter of a BJT in CE Configuration	EXPTNO:5
	DATE:

AIM : To Plot input and output Characteristics of BJT in Common Emitter Configuration And find input and output resistances.

APPARATUS:

1.TransistorBC107orSL100	1No.
2. Resistor1KΩ	1No.
3.Ammeter0-50mA,0-500µA	2No.
4.Voltmeter0-1V,0-30V	2No.
5.0-30V,1ADualChannelpowersupply	1No.
6.BreadBoard	1No.
7.Connectingwires	

THEORY:

In a common Emitter transistor Emitter terminal is connected common to both the input(Emitter–Base)voltageandtheoutput(Collector–Emitter)voltage.Voltmetersand Ammeters are connected to measure the input and output voltages and currents.

1**. Input Impedance (hie**): It is ratio of input base voltage (VBE) to the change in input base current(IB) with the output collector voltage (VCE) kept constant. It is the slope of the input characteristics IB vs VBE .

$$hie = \frac{\Delta V_{BE}}{\Delta I_B}, \; V_{CE} \text{ Constant} \quad (\Omega)$$

2.Reverse voltage gain (hre) : It is the ratio of the change in the input base voltage (VBE) and the Corresponding change in output collector(IC) voltage with constant input base current(IB).

It is the **slope VBE vs VCE curve**

$$hre = \frac{\Delta V_{BE}}{\Delta V_{CE}}, \; I_B \text{ constant}$$

3. **Forward Current Gain (hfe):** It is the ratio of the change in the output collector current(IC) to the corresponding change in the input base current (IB) keeping output collector voltage (VCE) constant. It is the slope of **Ic vs IB** curve .

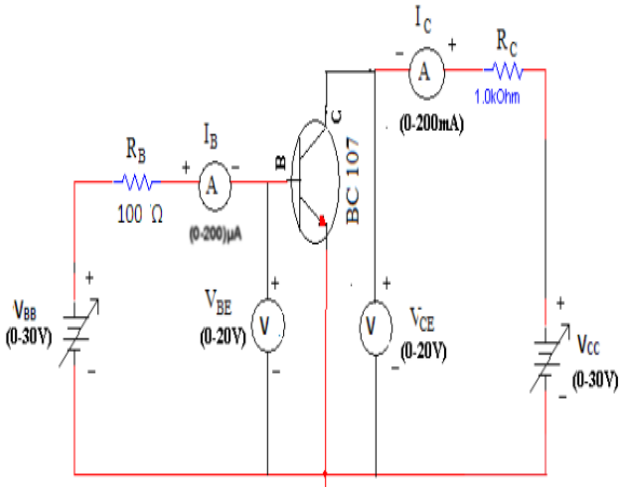
$$hfe = \frac{\Delta Ic}{\Delta I_B} \text{ , } V_{CE} \text{ Constant}$$

4. **Output Admittance (hoe):** It is the ratio of change in the output collector current (Ic) to the corresponding change in the output collector voltage(VCE) with the input base current (IB) kept constant. It is the slope of the output characteristics **VCE vs Ic**

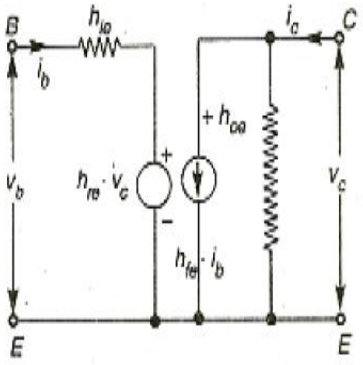
$$hoe = \frac{\Delta Ic}{\Delta V_{CE}} \text{ , } I_B \text{ constant} \qquad (\text{ ʊ })$$

.

CIRCUITDIAGRAM:



h – Parameter model of CE transistor:



Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CE} = 0V by varying V_{CC}.
3. Varying V_{BB} gradually, note down base current I_B and base-emitter voltage V_{BE}.
4. Step size is not fixed because of non linear curve. Initially vary V_{BB} in steps of 0.1V. Once the current starts increasing vary V_{BB} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CE} = 5V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current I_B = 20μA by varying V_{BB}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and Collector-Emitter Voltage(V_{CE}).
4. Repeat above procedure (step 3) for I_B = 60µA, 0µA.

INPUTCHARACTERISTICS

TABULARFORM:

S.No.	V_{CE}=0VOpen		V_{CE}= 1V	
	(V_{BE}V)	I_B(A)	V_{BE}(V)	I_B(□A)

OUTPUTCHARACTERISTICS:

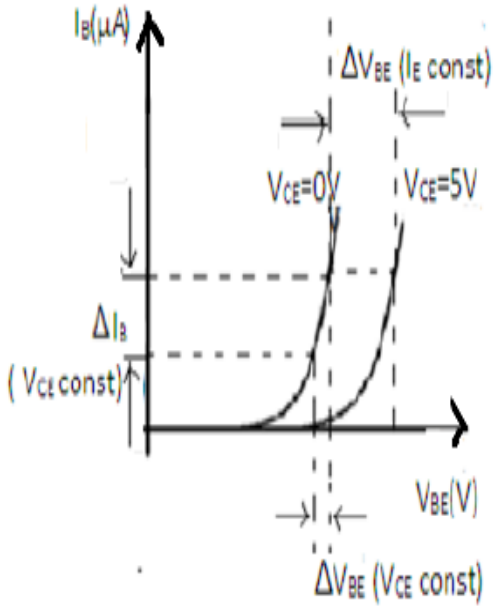
TABULARFORM:

S.No.	I_B=100□A		I_B=200□A	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)

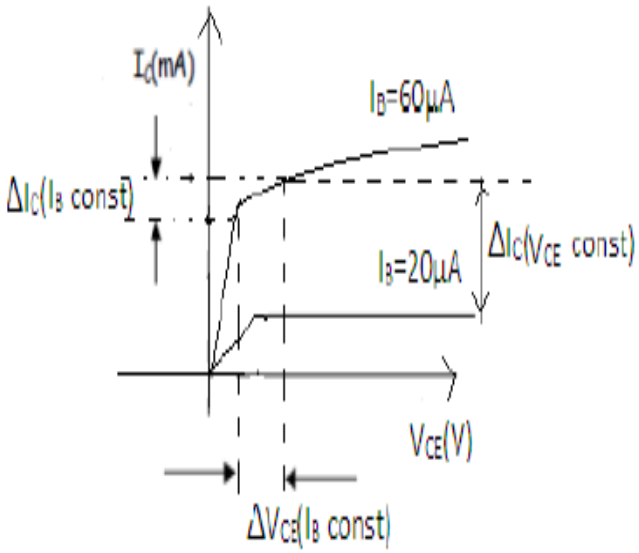
GRAPH:

1. Plot the input characteristics by taking I_B on Y-Axis and V_{BE} on X-Axis.
2. Plot the output characteristics by taking I_C on the Y-Axis and V_{CE} on X- Axis

Graph:



Input Characteristics



Output Characteristics

Calculations from Graph:

1. Input Characteristics: To obtain input resistance find ΔV_{BE} and ΔI_B for a constant V_{CE} on one of the input characteristics.
   Input impedance = $h_{ie} = R_i = \Delta V_{BE} / \Delta I_B$ (V_{CE} is constant)
   Reverse voltage gain = $h_{re} = \Delta V_{EB} / \Delta V_{CE}$ (I_B = constant)
2. Output Characteristics: To obtain output resistance find ΔI_C and ΔV_{CB} at a constant I_B.
   Output admittance 1/hoe = $R_o = \Delta I_C / \Delta V_{CE}$ (I_B is constant)
   Forward current gain = hfe = $\Delta I_C / \Delta I_B$ (V_{CE} = constant)

PRECAUTIONS:

1. Keep all COARSE controls of RPS minimum and CURRENT controls in maximum position before switch ON.
2. Carefully connect the transistor terminals.

Result:

The h-parameters for a transistor in CE configuration are:

a. The Input Resistance (h_{ie}) _____Ohms.
b. The Reverse Voltage Gain (h_{re}) _____.
c. The Output Conductance (h_{oe}) _____ Mhos.
d. The Forward Current Gain (h_{fe}) _____.

VIVAQUESTIONS:

1. Give the relation between I_B,$I_C$and I_E
2. Give the relation between I_{CEO} and I_{CBO}.
3. Define the transport factor.
4. Define saturation region, cut-off region and active region.

Determination of break over voltage of SCR using V-I Characteristics	EXPTNO:6
	DATE:

AIM: ToobtainV-Icharacteristicsandtofindon-stateforwardresistanceofgivenSCR.To determine holding, latching current and break over voltage of given SCR.

APPARATUS REQUIRED : Trainer kit, Patch cards Multi meters.

THEORY : An SCR is a three-terminal, three-junction, and four-layer semiconductor device that is used to perform switching functions in power circuits. Sometimes the SCR is also called as Thyristor.

When Gate is Open Circuited

When no voltage applied to gate terminal, junction J2, is reverse biased and the junctions J1 and J3 are forward biased. Since one of the three junctions is reverse biased so there is no current can flow through the load, hence the SCR is OFF. However, if the applied voltage is gradually increased, a stage is reached, when reverse biased junction (J2) breaks down. The SCR now, starts conducting and become ON. The value of applied voltage at which the reverse biased junction breaks down and the SCR becomes ON is known as Break over Voltage.

When Gate is Positive with Respect to Cathode

The SCR can be turned ON at smaller applied voltage by the application of a small positive voltage at the gate terminal. When gate voltage is applied the junction J3 is forward biased and junction J2 is reverse biased. Thus, the electrons from n – type layer starts moving across the junction J3 toward p –type material and the holes from p –type material towards the n – type material. Due to the movement of holes and electrons across the junction J3 the gate current starts flowing. Because of gate current the anode current increases. The increased anode current makes the more electrons available at the junction J2. As a result of this process, in a small time, the junction J2 breaks down and the SCR is turn ON.

CIRCUITDIAGRAM:

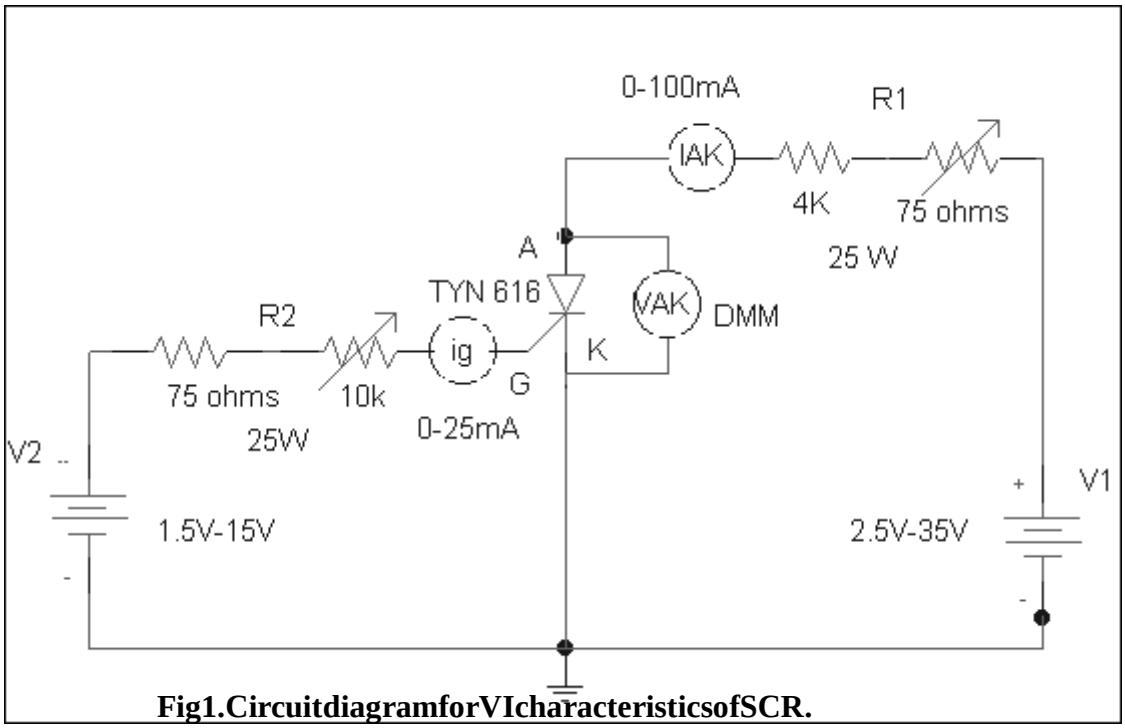


Fig1.CircuitdiagramforVIcharacteristicsofSCR.

Characteristiccurve:

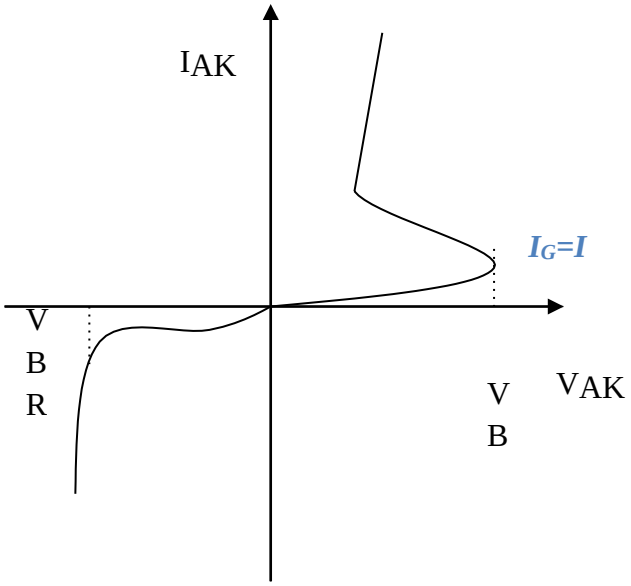


Fig2:StaticcharacteristicofSCR.

TABULAR COLUMN:

Gate current $I_G=I_{G1}=$…..mA

V_{AK}(Volts)	I_{AK}(mA)

PROCEDURE:

- Connections are made as shown in the circuit diagram.
- Set R_1 and R_2 to mid position and V_1 and V_2 to minimum
- Set the gate current $I_G = I_{G1}$ (such that forward break over voltage is between 15 to 20V), by varying R_2 and V_2.
- Slowly vary V_1 in steps of 2V and note down V_{AK} and I_{Ak} at each step till SCR conducts. (Note down maximum V_{AK}, which is forward break over voltage just before SCR conducts).

***FINDINGLATCHINGCURRENT**:*

- Ensure that the SCR is in the state of conduction.
- Start reducing (V_{AK}) anode voltage in steps of 2V; simultaneously check the state of SCR
- by switching off gate supply V_2. If SCR switches off just by removing gate terminal,
- and switches on by connecting gate supply, then the corresponding anode current
- I_A is the latching current(I_L) for the SCR.

FINDINGHOLDINGCURRENT:

- Ensure that the SCR is in the state of conduction.
- Switch off the gate supply permanently.
- Start reducing (V_{AK}) anode voltage in steps of 2V; simultaneously check the state of SCR.
- If SCR switches off. Note down the anode current (I_A) just before it drops to zero, Which will be I_H.
- Reverse the anode voltage polarity.
- Vary V_{AK} in steps of 5V till 25V and note down V_{AK} and I_A values at each step
- Plot forward and reverse characteristics using the above-tabulated values. Find the SCR Forward resistance using the graph.
- Repeat the above procedure for the forward and reverse characteristics of SCR for a gate Current $I_g = I_{g2}$.

RESULT: The values of V_{AK} and I_{AK} are verified.

UJT CHARACTERISTICS	**EXPTNO:7**
	DATE:

AIM: To obtain the V-I characteristics of UJT and plot its input negative resistanceCharacteristics also to find its Intrinsic Standoff Ratio

APPARATUS:

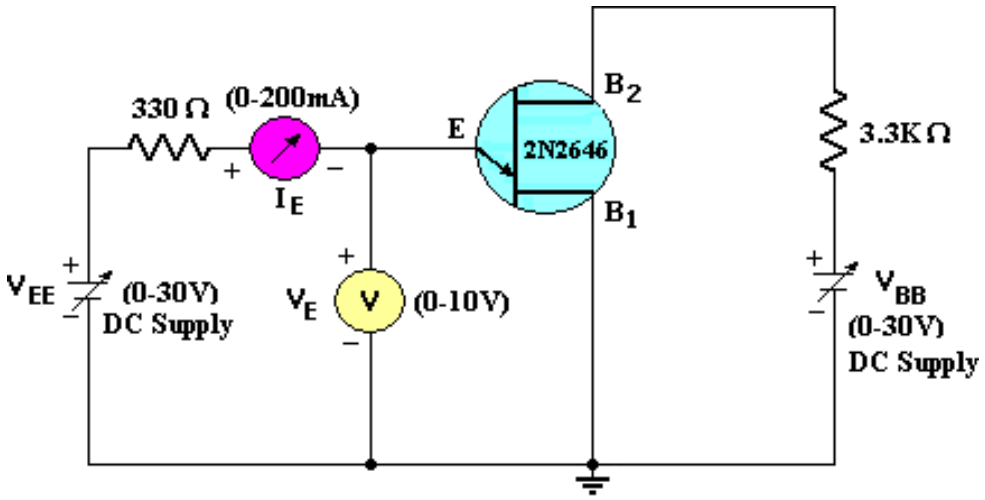
S.No	Name	Range/Value	Quantity
1	Power supply	(0–30V)	1
2	Transistor	UJT2N2646	1
3	Resistors	3.3KΩ,330Ω	Each1
4	Ammeter	(0-100mA)	1
5	Voltmeter	(0–10V)	1
6	Bread Board and connecting wires	-	1Set

Theory:

A Uni junction Transistor (UJT) is an electronic semiconductor device that has only one junction. It has three terminals an emitter (E) and two bases (B1 and B2). The base is formed by lightly doped n-type bar of silicon. Two ohmic contacts B1 and B2 are attached at its ends. The emitter is of p-type and it is heavily doped. The resistance between B1 and B2, when the emitter is open-circuit is called inter base resistance. The original UJT, is a simple device that is essentially a bar of N type semiconductor material into which P type material has been diffused somewhere along its length.

The UJT is biased with a positive voltage between the two bases. This causes a potential drop along the length of the device. When the emitter voltage is driven approximately one diode voltage above the voltage at the point where the P diffusion (emitter) is, current will begin to flow from the emitter into the base region. Because the base region is very lightly doped, the additional current(actually charges in the base region) causes (conductivity modulation) which reduces the resistance of the portion of the base between the emitter junction and the B2 terminal. This reduction in resistance means that the emitter junction is more forward biased, and so even more current is injected. Overall, the effect isa negative resistance at the emitter terminal. This is what makes the UJT useful, especially in simple oscillator circuits. When the emitter voltage reaches Vp, the current starts to increase and the emitter voltage starts to decrease. This is represented by negative slope of the characteristics which is referred to as the negative resistance region, beyond the valley point , V_{EB} proportional to I_E.

CIRCUITDIAGRAM:



UJT Characteristics

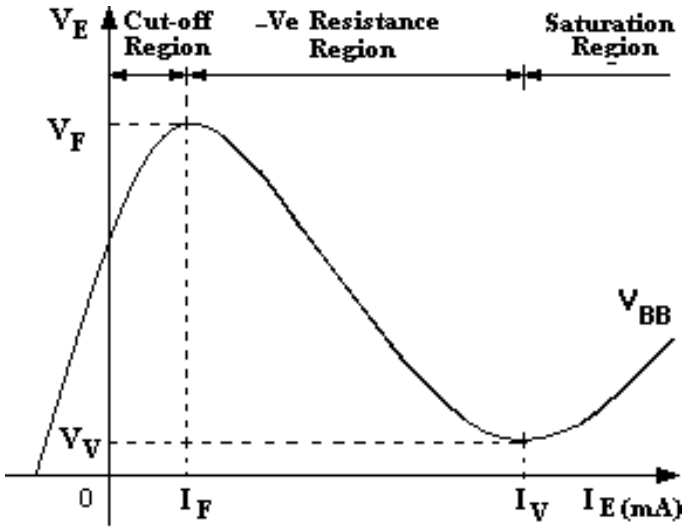
PROCEDURE:

1. Connect the circuit as shown in above figure.
2. Keep V_{BB}=5V, Vary V_{EE} smoothly with fine control such that V_E Varies in steps of 0.5volts from zero and note down the resulting emitter current I_E for each step in the tabular form.
3. Repeat the experiment for V_{BB}=7V and for V_{BB}=10V.
4. Draw the graph between V_E Vs I_E by keeping V_{BB} constant.

TABULARFORM:

V_{BB}=5V		**V_{BB}= 7V**		**V_{BB}= 10V**	
Vs (volts)	**I_E (mA)**	**Vs (volts)**	**I_E (mA)**	**Vs (volts)**	**I_E (mA)**

MODELGRAPH:



UJT Characteristics

VIVAQUESTIONS:

1. What are the applications of UJT?
2. Why UJT is called as a Relaxation Oscillator?
3. Which type of switch is used in UJT?
4. What is Intrinsicst and off ratio?
5. Why UJT is called a negative resistance device?
6. Draw the circuit schematic for UJT?
7. What are the applications of UJT in triggering circuits?
8. Write the equation for Intrinsicst and off ratio?
9. Define valley voltage in UJT?
10. How UJT can be used for firing the silicon controlled rectifiers?
11. What are applications of UJT in Bi stable circuits?
12. What is the main application of UJT?

RESULT: Thus, we obtained the V-I characteristics of UJT and plotted its input negative resistance Characteristics also found its Intrinsic Standoff Ratio.

Estimation of Stability factor for a transistor self-biasing circuit.

EXPTNO:8

DATE:

AIM : Design a Self Bias Circuit For the following Specifications
Icq=5mA,Vceq=6.0V,Vcc=12.0V,Rc=1KΩ,S=25.

Find the quiescent point (Operating Point) values of I_{CQ} and V_{CEQ} from the experiment and to find the maximum signal handling capability of the Amplifier.

APPARATUS:

S.No	Name	Range/ Value	Quantity
1	Dual Regulated D.C Power supply	0–30Volts	1
2	Transistor	BC107	1
3	Capacitors	50µf	2
4	Capacitors	10µf	1
5	Multi meter	-	1
6	Signal Generator	(0–1MHz)	1
7	Bread Board and connecting wires	-	1Set
8	Dual Trace CRO	20MHz	1

THEORY:

A transistor acts as an amplifier in active region. Biasing circuit is used in a transistor to keep in the active region. Following are the three common biasing circuits used in transistors.

1) Fixed bias circuit:- It is named so because it provides a fixed value of base current for given values of VCC and Rb.

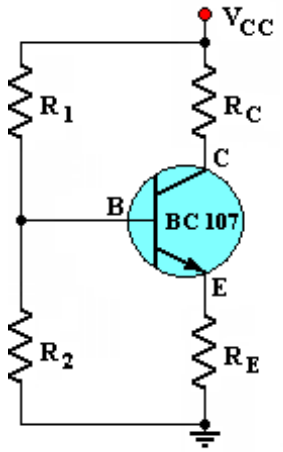
2) Collector to base bias circuit:- In this circuit the base bias is taken from the collector by connecting a resistor between base and collector.

3) Self bias circuit:- In this circuit the base bias is obtained by using a voltage divider network. An emitter resistor is used to limit the collector current and hence the Q-point is stable.

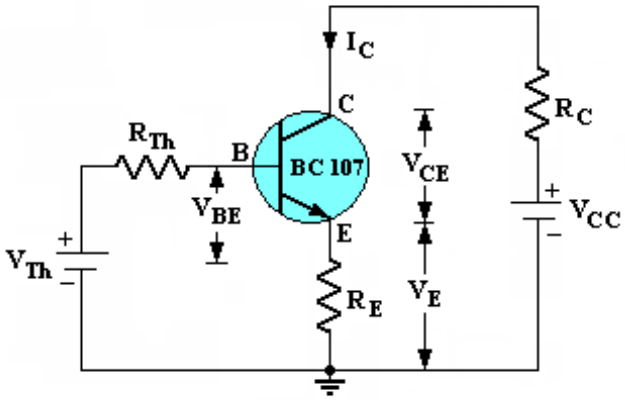
Stability factor is defined as the rate of change of collectorcurrent with reverse saturation current. For a stable Q-point stability factor should be as small as possible. A self bias circuit provides the least stability factor out of all the configurations and hence it is commonly preferred over other biasing circuits. Stability factor is mathematically given by the following **equation**

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta \times \frac{\partial IB}{\partial IC}}$$

CIRCUIT DIAGRAMS:



Self Bias circuit



Self Bias equivalent circuit

DESIGNPROCEDURE:

c) Design a self bias circuit for which the biasing conditions are as follows. V_{CC} = 12V, I_C = 1mA, V_{CE} = 6V and Stability factor is S = 10. Use R_C = 4.7KΩ. Use a transistor with β = 200 and V_{BE} = 0.65V.

Solution: Use, $I_C = \beta \times I_B$

$\Rightarrow I_B = 5\mu A$

Apply KVL to the output loop:

$-V_{CC} + I_C \times R_C + V_{CE} + I_C \times R_E = 0$

$\Rightarrow R_E = 1.3K\Omega$

Apply Thevenin's theorem to the base circuit, then

$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$ And $R_B = \frac{R_1 \times R_2}{R_1 + R_2}$

We know that the stability factor for a self bias circuit is given by,

$$S = \frac{1+\beta}{1+\frac{\beta \times R_E}{R_B + R_E}}$$

$$\Rightarrow R_B = 12.31K\Omega$$

Apply KVL to the input loop, then

$$-V_B + I_B \times R_B + V_{BE} - I_E \times R_E = 0$$

$$\Rightarrow V_B = 2.01\text{V}$$

Divide R_B with V_B:

$$\Rightarrow R_1 = \frac{V_{CC} \times R_B}{V_B} = 73.5K\Omega$$

Also, $R_B = \frac{R_1 \times R_2}{R_1 + R_2} \quad \Rightarrow R_2 = 14.8K\Omega$

PROCEDURE:

1. Connectthecircuitasperthecircuitdiagram.ApplyVccof12VoltsDC.
2. Find the resulting DC Values of Icq and Vceq.
3. Applya1KHzsignalfromtheSignalGeneratorandobservetheO/P on CRO.
4. IncreasetheI/Pvoltageslowlyuntiltheoutputwaveformstartsdistortion
5. NotedowntheinputvoltageViatthepointwheretheoutputstartsdistortion
6. This input value is known as maximum signal handling capability.
7. Calculate the gain of the amplifier.

PRECAUTIONS:

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

VIVAQUESTIONS:

1. What is meant by Self Bias & fixed Bias circuits, Which one is preferred and why?
2. What is the significance of Emitter Resistance?
3. What is stability factor?
4. What is DC Load line and A.C .Load line?
5. What is quiescent point? What are the various parameters of the transistor that cause drift in q-point?
6. What are different techniques of stabilization?
7. Relate stability factor with the circuit parameters
8. What is the relation between α and β.

9. If bypass capacitor is removed ,what happens to the gain?

RESULT:

Stability factors are calculated for self bias circuit. Theoretical and practical values of the stability factor S is verified.

FET Characteristics	EXPTNO:9
	DATE:

AIM: 1.To plot drain Characteristics and Transfer Characteristics of Field Effect Transistor
2. To analyze drain resistance, transconductance and amplification factor.

APPARATUS:

1. FET :	1 No.
2. Connecting Wires	
3. Ammeter 0 – 20 mA	1 No.
4. Multi meter (Voltmeter 0-10v)	2 No.
5. Dual Channel Power Supply(0-30V)	1 No.
6. Bread Board	1 No.
7.Connectging Wires	One Bunch

THEORY:

A Junction Field Effect Transistor(JFET) consists of a P – type or N – type silicon bar. The bar is the conducting channel for the charge carriers. If the bar is made up of N- type material it is known as N- channel FET and if the bar is made up of P- type material it is known as P- channel FET. To form a JFET two junction diodes are connected internally. These are three terminals in FET, namely Source, GATE, and Drain GATE is the common terminal to both input and output.

DRAIN CHARACTERSTICS:-

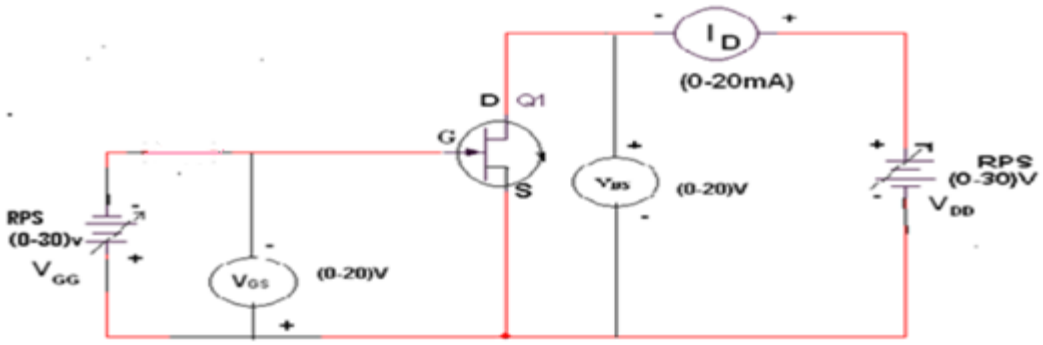
This is the curve drawn between the drain – source voltage (V_{DS}) and the drain current (I_D) at constant gate source voltage. The drain current I_D rises rapidly with drain source voltage V_{DS}, reaching some value, it becomes constant.

TRANSCONDUCTANCE:(g_m) $=\Delta I_D/\Delta V_{GS}$ At constant V_{DS}

DRAINRESISTANCE:(rd) $= \Delta V_{DS}/\Delta I_D$ At constant VGs

AMPLIFICATION FACTOR: (μ) $= r_d * g_m$

CIRCUIT DIAGRAM:



PROCEDURE:

OUTPUT (Drain) CHARACTERISTICS

1. Connect the circuit as shown in the diagram.
2. Make V_{GS} =0v, by adjusting (Channel – I) power supply.
3. Adjust the 0 – 30v (Channel – II) power supply and note the values of I_D and V_{DS} with the variation of V_{DS} in step of 1V, as per table given below.
4. Repeat the above procedure for V_{GS}=-0.5v and -1v.

TABULAR FORM (DRAIN OR OUTPUT CHARACTERISTICS):

V_{GS} =		V_{GS} =		V_{GS} =	
V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

PROCEDURE:

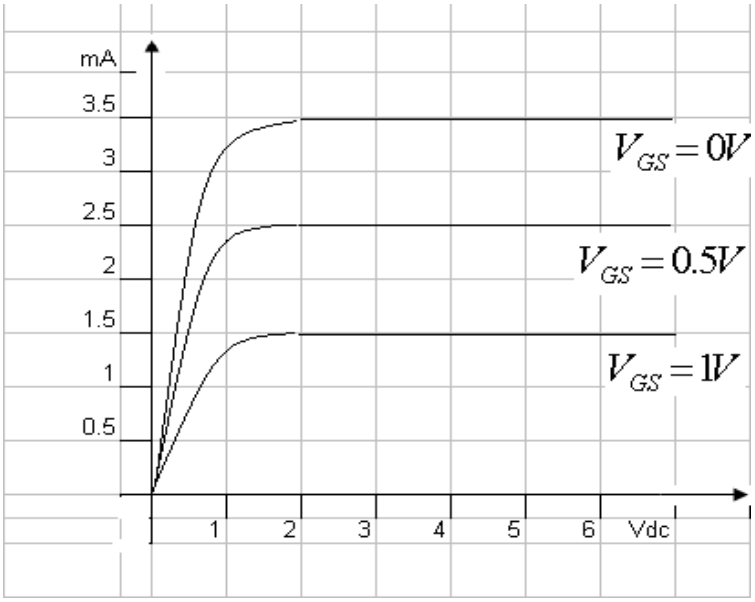
INPUT (Transfer) CHARACTERISTICS

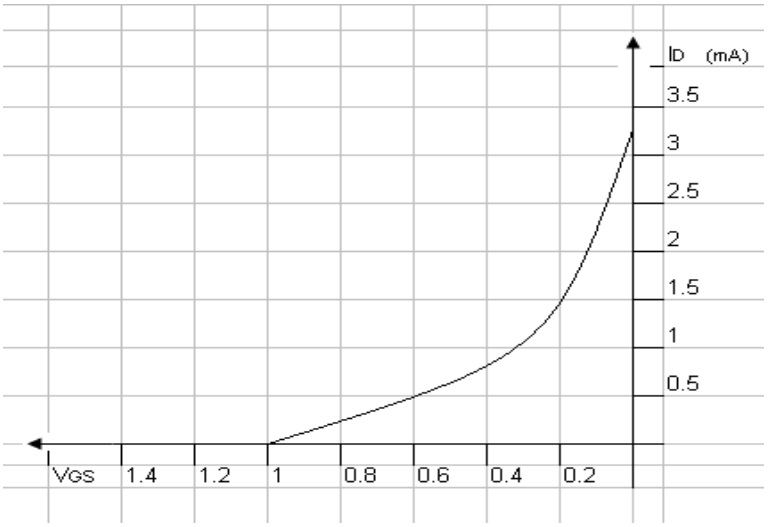
1. Connect the circuit as shown in the diagram.
2. Make V_{GS} =1v, by adjusting 0 – 30v (Channel – II) power supply
3. Adjust the 0 – 5v (Channel – I) power supply and note the values of I_D and V_{DS} with the variation of V_{GS} in step of 0.2v, as per table given below.
4. Repeat the above procedure for V_{DS}=1.5v and2v.

TABULAR FORM (TRANSFER OR INTPUT CHARACTERISTICS):

V_{DS}=		V_{DS} =		V_{DS} =	
V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)	V_{GS}(V)	I_D(mA)

DRAINOROUTPUT CHARACTERISTICS





TRANSFER OR INPUT CHARACTERISTICS

GRAPH:

1. Plot the Output Characteristics by taking I_D on Y-axis and V_{DS} on X-axis for constant values of V_{GS}
2. Plot the Transfer Characteristics by taking I_D on Y-axis and V_{GS} on X-axis for constant values of V_{DS}

PRECAUTIONS:

1. Keep all COARSE & FINE controls of RPS minimum and CURRENT controls in maximum position before switch ON.
2. Carefully connect the FET terminals.

RESULT: Thus the Drain & Transfer Characteristics of the given JFET are studied and the following parameters are found.

1. TRANSCONDUCTANCE :
2. DRAIN RESISTANCE :
3. AMPLIFICATION FACTOR :

VIVA QUESTIONS:

1. Define Transfer characteristics of FET.
2. Define Drain characteristics of FET.
3. Define Trans conductance.

Design of Common Emitter AMPLIFIER	EXPTNO:10
	DATE:

AIM: To determine Gain and Bandwidth of CE amplifier from frequency response.

APPARATUS: -

S. No.	Name	Range	Quantity
1.	Transistor	BC 107	1
2.	Resistor	1kΩ,33kΩ,3.3kΩ	4,1,1
3.	Capacitor	10μF, 100μF	2, 1
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1
8.	Connecting wires		

Theory:

Frequency response of an amplifier is defined as the variation of gain with respective frequency. The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at lower cut-off frequency and remains constant till higher cut-off frequency and then it falls again as the frequency increases.

At low frequencies the reactance of coupling capacitor C_C is quite high and hence very small part of signal will pass through from one stage to the next stage.

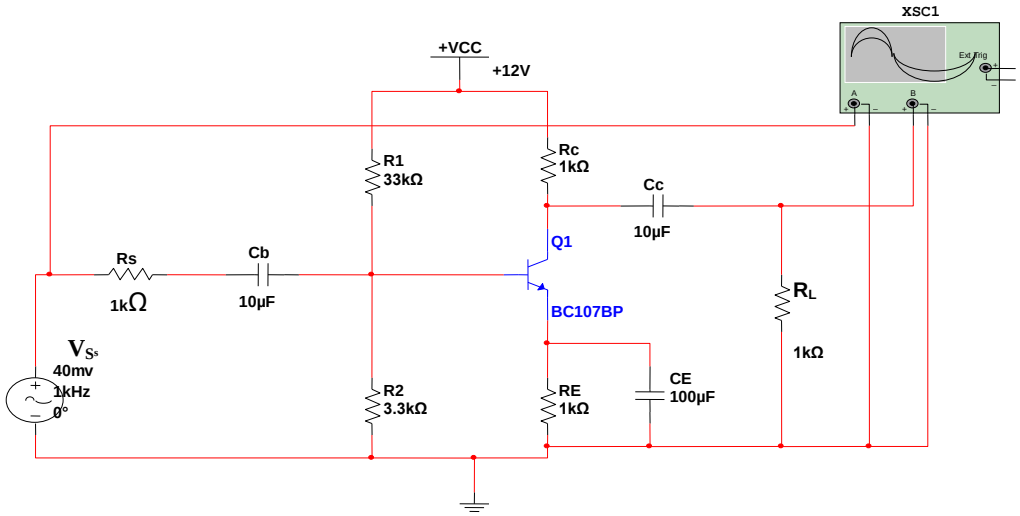
At high frequencies the reactance of inter electrode capacitance is very small and behaves as a short circuit. This increases the loading effect on next stage and service to reduce the voltage gain due to these reasons the voltage gain drops at high frequencies.

At mid frequencies the effect of coupling capacitors is negligible and acts like short circuit, whereas inter electrode capacitors acts like open circuit. So, the circuit becomes resistive at mid frequencies and the voltage gain remains constant during this range.

The gain is more stable in common emitter amplifier without bypass capacitor compared to with bypass capacitor.

CIRCUIT DIAGRAM:-

With emitter bypass capacitor Ce



PROCEDURE:

1. Connect the circuit on bread board as shown in the circuit diagram.

2. By keeping the amplitude of the input signal constant vary the frequency from 0 to 1MHZ.

3. Note down the amplitude of the output signal for corresponding values of input frequencies.

4. Calculate the voltage gain in decibels.

5. Plot in semi-log graph between gain versus frequency and calculate the band width.

OBSERVATIONS:

Input Voltage V_{IN} = -----

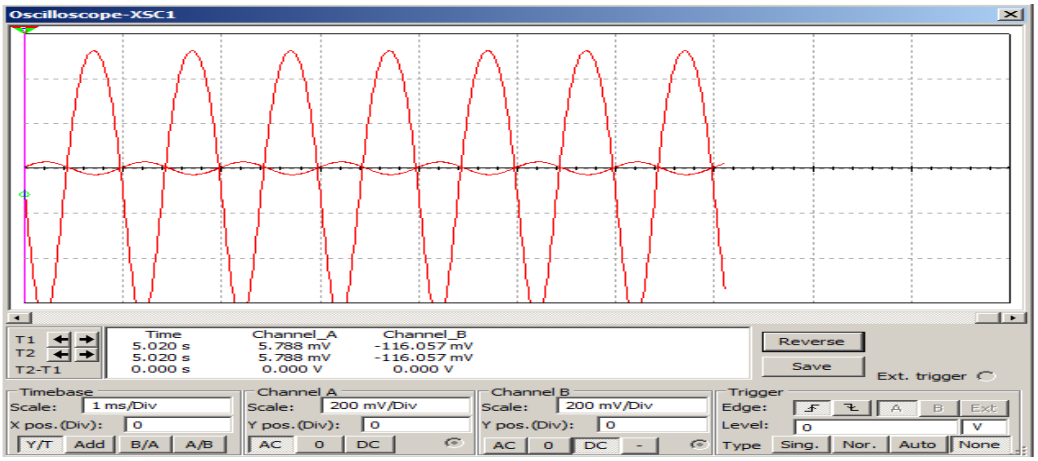
S.NO	FREQUENCY	V_{OUT}	GAIN(Av) = V_{OUT}/V_{IN}	GAIN in dB=20log Av

CALCULATIONS:

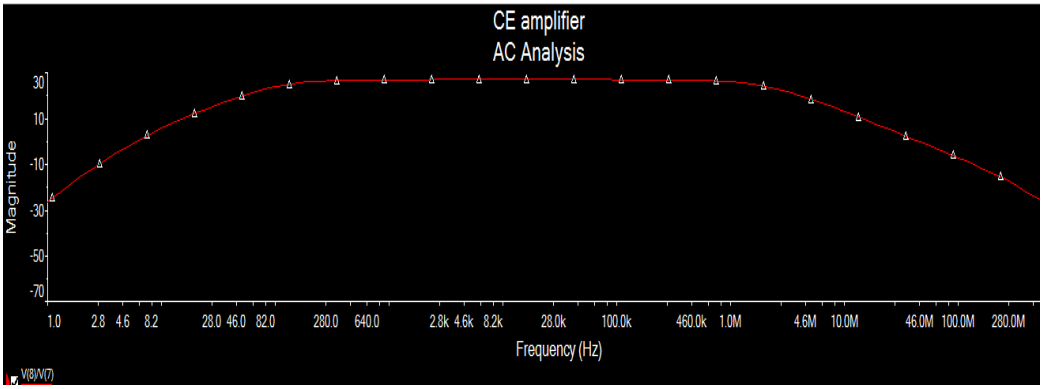
i. Determine lower cut-off frequency and upper cut-off frequency from the graph.

ii. Calculate Band width.

Expected waveforms:



GRAPH:



PRECAUTIONS:

1. Test Transistors before assembling the circuits

2. Resistors should be connected properly without interchanging the values.

3. Check the continuity of the connecting wires.

APPLICATIONS:

1. Audio amplifiers

2. Radio Transmitters and Receivers.

RESULT:

i. Lower cut-off frequency =

ii. Upper cut-off frequency =

iii. Band width =

Viva Questions:-

1. Define Bandwidth of an amplifier?

2. What is the importance of Cc capacitor in CE amplifier?

3. Mention the purpose of C_b capacitor in CE amplifier?

4. What is the effect of Ce on gain & bandwidth of CE amplifier?

5. What is the amount of phase shift in CE amplifier?

6. List the applications of CE amplifier?

Design of FET-CS Amplifier	EXPTNO:12
	DATE:

Aim: To determine Gain and Bandwidth of CS FET amplifier from frequency response.

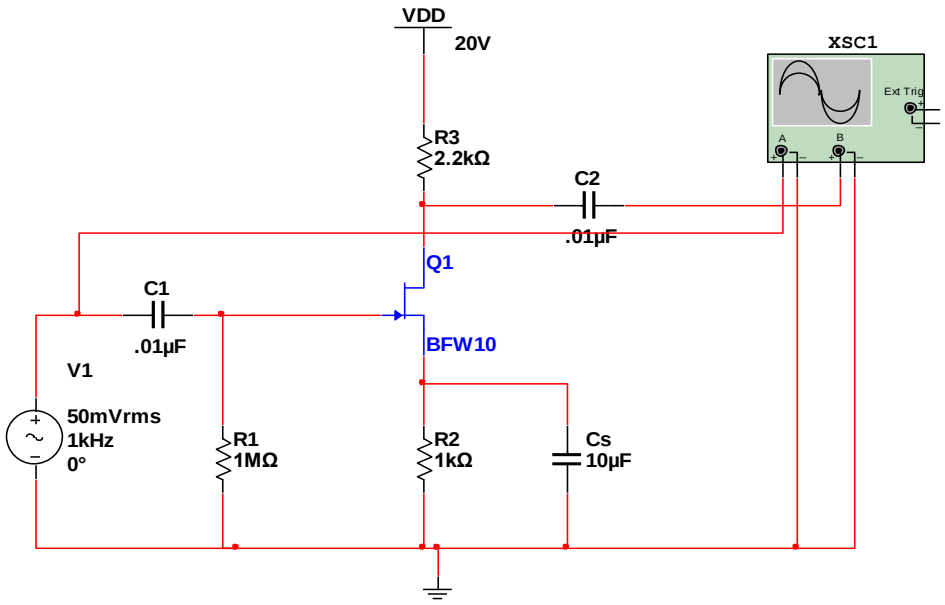
.**Apparatus Required:**

S. No.	Name	Range	Quantity
1.	FET transistor	BFW10	1
2.	Resistor	1 kΩ,1MΩ,2.2KΩ	1,1,1
3.	Capacitor	10μF, 100 μF	2,1
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1
8.	Connecting wires		

THEORY:

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources.The self-bias configuration requires only one dc supply to establish the desired operating point.The capacitor CS across the source resistance assumes it's short-circuiting equivalence for dc,allowing RS to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of RS.

Circuit diagram:-



PROCEDURE:

1. Connect the circuit on bread board as shown in the circuit diagram.
2. By keeping the amplitude of the input signal constant, vary the frequency from zero to 1 MHz
3. Note down the amplitude of the output signal for corresponding values of input frequencies.
4. Calculate the voltage gain in decibels.
5. Plot in semi-log graph between gain versus frequency and calculate the band width.

OBSERVATIONS:

Input voltage $\mathbf{V_{IN}}$ = -----

S.NO	FREQUENCY	V_{OUT}	GAIN(Av) =	GAIN in

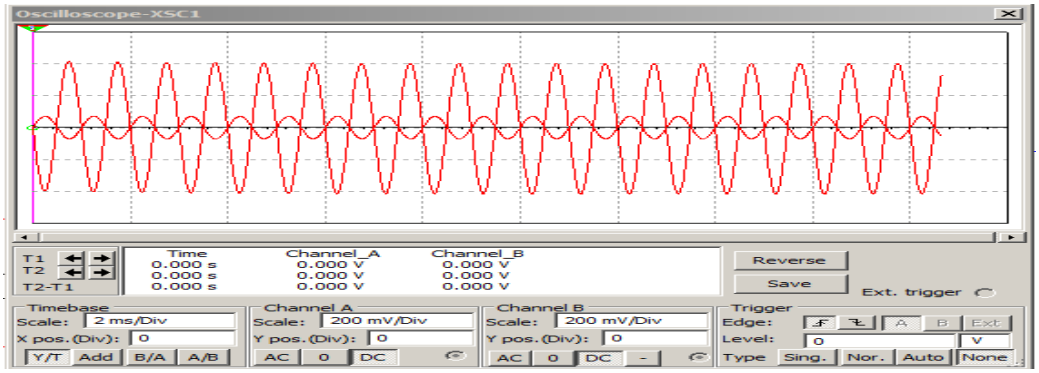
			V_{OUT}/V_{IN}	dB=20log Av

CALCULATIONS:

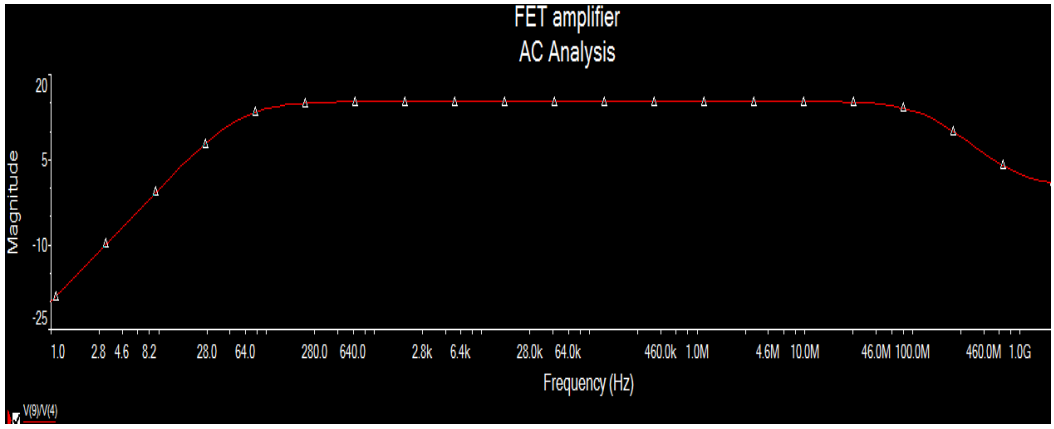
i. Determine lower cut-off frequency and upper cut-off frequency from the graph.

ii. Calculate Band width.

Expected wave forms:



Graph:



PRECAUTIONS:

1. Test Transistors before assembling the circuits
2. Resistors should be connected properly without interchanging the values.
3. Check the continuity of the connecting wires.

APPLICATIONS:

The applications where we need high input impedance.

RESULT:

i. Lower cut-off frequency =
ii. Upper cut-off frequency =
iii. Band width =

Viva Questions:-

1. Draw the FET small signal model.
2. Why input impedance of FET is high?
3. What is the current gain of CS amplifier?
4. What is the voltage gain of CS amplifier?